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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/648,038	08/26/2003	Alexander E. Andreev	03-0933/L13.12-0240	2425

7590

06/19/2006

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EXAMINER

CHAUDRY, MUJTABA M

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 06/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

DETAILED ACTION

Election/Restrictions

Examiner makes acknowledgement to Applicants election of claims 1-9 without traverse. Applicants are reminded to cancel non-elected claims 10-20 in subsequent communication. Claims 1-9 are considered on the merits.

Information Disclosure Statement

The references listed in the information disclosure statement (IDS) submitted on August 27, 2003 have been considered. The submission is in compliance with the provisions of 37 CFR 1.97.

Oath/Declaration

The Oath filed February 18, 2003 complies with all the requirements set forth in MPEP 602 and therefore is accepted.

Drawings

The drawings are objected to because:

- Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page

header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

- Figure 2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Appropriate correction is required.

Specification

Applicant is reminded of the proper language and format for an abstract of the disclosure.

- On page 1, line 26 the word "in" should be capitalized (i.e. In).
- The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors.

Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Allowable Subject Matter

Claims 2-4 and 6-9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The issues under 35 USC 112 would need to be addressed and corrected as well.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1 and 5 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

- It is not clear what the Applicants intend to mean with, "...a **first p/2 group of the modules...**" when p is previously defined in the claim as the number of inputs and number of outputs.
- The subsequent limitation of, "...coupled to **the n inputs...**" There is no antecedent for this limitation. Is n the same as p or different?
- It is not clear what the Applicants intend to mean with, "...a **second p/2 group of the modules...**" when p is previously defined in the claim as the number of inputs and number of outputs.
- It is not clear what the Applicants intend to mean with, "...a **respective permutation...**" when respective is a relative term.

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Appropriate correction is required.

Claim Rejections - 35 USC § 103

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35

U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

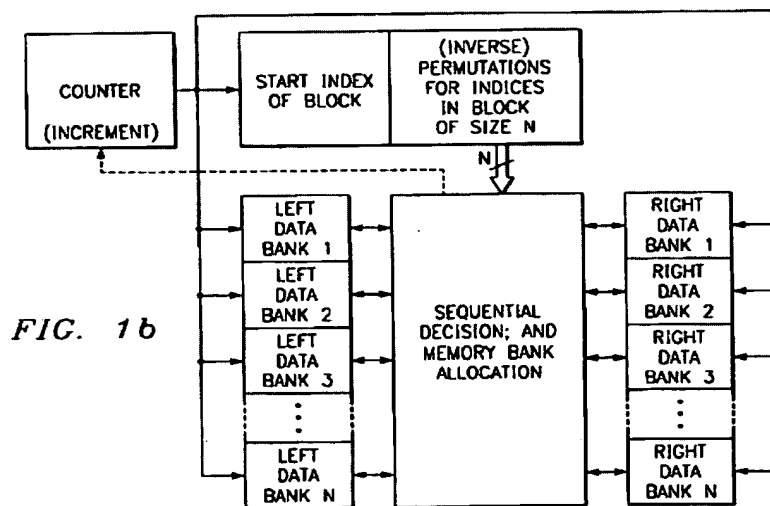
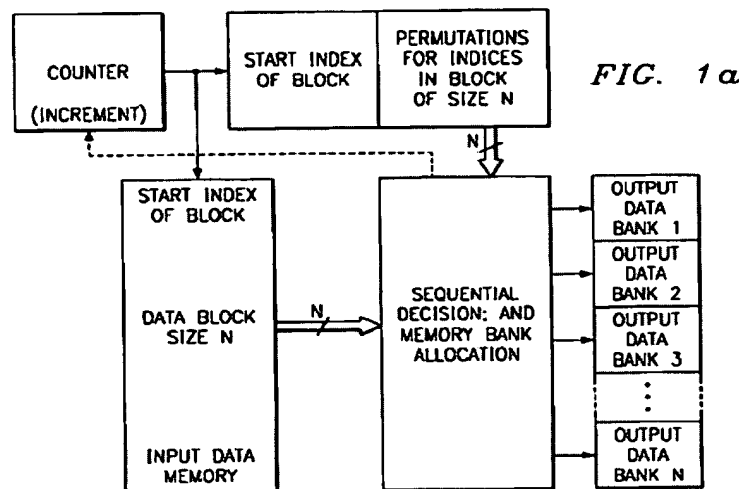
Claims 1 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gatherer et al.

(USON 6603412) further in view of Models of Computation (by John E. Savage pages 309-311, Applicants' IDS).

As per claim 1, Gatherer et al. (herein after: Gatherer) substantially teaches (Figures 1a and 1b) a quasi-parallel read/write interleaver architecture for data blocks by sequential spreading of variable size data subblocks into memory banks with bank address contention initiating the next data subblock. Iterative Turbo decoders with MAP decoders use such quasi-parallel interleavers and deinterleavers. In particular, in a preferred embodiment, Gatherer teaches interleavers to permute data by reading in chunks of data and writing in parallel into banks up to an address contention at a bank. The larger the number of banks (and corresponding write circuits), the larger the chunk size and the greater the average number of parallel writes.

Gatherer does not explicitly teach a plurality of modules where each has two inputs and two outputs as stated in the present application.

However, Savage teaches, in an analogous art, (page 310, Figure 7.20) a plurality of modules wherein each has two inputs and two outputs. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to use multiple modules with two inputs and two outputs within the teaching of Gatherer. This modification would have been obvious to one of ordinary skill in the art because one of ordinary skill would have recognized that by having multiple modules with two inputs and outputs would have increased efficiency as stated by Savage (page 311).



As per claim 5, Gatherer teaches (Figures 1a and 1b) a quasi-parallel read/write interleaver architecture for data blocks by sequential spreading of variable size data subblocks into memory banks with bank address contention initiating the next data subblock. Iterative Turbo decoders with MAP decoders use such quasi-parallel interleavers and deinterleavers. In particular, in a preferred embodiment, Gatherer teaches interleavers to permute data by reading in chunks of data and writing in parallel into banks up to an address contention at a bank. The larger the number of banks (and corresponding write circuits), the larger the chunk size and the greater the average number of parallel writes.

Gatherer does not explicitly teach a plurality of modules where each has two inputs and two outputs as stated in the present application.

However, Savage teaches, in an analogous art, (page 310, Figure 7.20) a plurality of modules wherein each has two inputs and two outputs. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to use multiple modules with two inputs and two outputs within the teaching of Gatherer. This modification would have been obvious to one of ordinary skill in the art because one of ordinary skill would have recognized that by having multiple modules with two inputs and outputs would have increased efficiency as stated by Savage (page 311).


Conclusion


The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Additional pertinent prior arts are included herein for Applicant's review.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mujtaba K. Chaudry whose telephone number is 571-272-3817. The examiner can normally be reached on Mon-Thur 9-7:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


Mujtaba Chaudry
Art Unit 2133
June 8, 2006


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